REMARKS

Claims 1-21 are pending in this application. Claims 22-38 were previously withdrawn. Claims 1 and 17 have been amended. No new matter has been added.

Claim 1 stands objected to because "there is insufficient antecedent basis for the limitation 'said substrate.'" (Office Action at 3). Claim 1 has been amended to correct this informality. Claim 17 stands objected to because "the limitation of said first conductors being N-type is unclear." (Office Action at 3). Claim 17 has been amended to correct this informality.

Claims 1-5 and 7-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Moise et al., U.S. Patent No. 6,534,809 ("Moise") in view of Jeng et al., U.S. Patent No. 5,839,734 ("Jeng"). This rejection is respectfully traversed.

The present invention relates to a method of forming an integrated circuit, such as a dynamic random access memory (DRAM) cell, which uses a metal plug structure for contacting source/drain regions of transistors located in the peripheral logic area of the circuitry. The metal plug structure is formed after high temperature processing of other structures, specifically, the capacitors in the memory array area, on the wafer.

Accordingly, amended independent claim 1 recites a "method of forming a memory device" by *inter alia* "forming metal plugs down to active areas of a substrate after heat treating said capacitor structure, wherein at least a portion of said metal plugs formed down to said active areas are for both N-channel and P-channel peripheral logic transistors of a semiconductor substrate located outside said memory array area containing said memory cell." Similarly, independent claim 2 recites a method of forming a memory device" by *inter alia*, "after said heat treating operation, forming an upper electrode layer in contact with said dielectric layer; and after forming said upper electrode layer, forming metal contacts contiguous to active areas of each of an N-channel and P-channel transistor in a peripheral logic area."

Independent claim 3 recites a method of fabricating metallized plugs in a memory device" by *inter alia* "defining multiple plug openings in material layers over said substrate at said periphery circuitry area of said substrate, wherein at least one of said plug openings exposes an active area of said transistor having said first conductivity type and at least one of said plug openings exposes an active area of said transistor having said second conductivity type; and forming a metal layer over said substrate and into said plug openings to contact said active areas after said heat is applied to said memory cell array area."

Independent claim 7 recites a "method of forming a memory device" by *inter alia* "forming at least portions of capacitors associated with said access transistors in said memory cell array area," "heat treating said capacitor portions," and "after said heat treating, forming first metal conductors which contact with active areas of said N-channel and P-channel peripheral logic transistors." Finally, independent claim 18 recites a "method of forming a memory device" by *inter alia* "heat treating said container capacitors," "forming N-channel and P-channel peripheral logic transistors outside said memory cell array area" and "forming peripheral metal plugs through said second insulating layer to contact each of said N-channel and P-channel peripheral logic transistors after said heat treating."

The subject matter of claims 1-5 and 7-19 would not have been obvious over Moise in view of Jeng. Specifically, the Office Action does not establish a *prima facie* case of obviousness. Courts have generally recognized that a showing of a prima facie case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573 (Fed. Cir. 1996).

Moise relates to a method of fabricating a ferroelectric memory (FeRAM) having ferroelectric capacitors that include hardmasks. (Col. 4, line 51-Col. 6, line 26). The focus of Moise is "creating the ferroelectric capacitors in a FeRAM process module that occurs between the front end module (defined to end with the formation of tungsten, which has the chemical symbol W, contacts) and backend process module (mostly metallization)." (Col. 4, lines 55-59).

The Examiner asserts that Moise teaches "[f]orming peripheral metal plugs 136 through the second insulating layer 134 to contact the N-channel or P-channel peripheral logic transistor after the heat treating." (Office Action at 4). The Applicants, however, respectfully submit that Moise does not provide such a teaching or suggestion. Instead, Moise teaches the formation of "contacts to the substrate," specifically plugs 114, in a FeRAM portion 103 and a region 105 prior to the formation or heat treatment of the capacitors. Moise teaches that plugs 114 are formed prior to the formation of the capacitors as part of step 202, a front end module. (Col. 7, lines 39-46; FIG. 2). Moreover, in FIG. 1, Moise shows each of plugs 114 contacting a region 110, which is shown above and in contact with a source/drain region 108. Moise, however, fails to specifically teach what region 110 is.[1]

The Examiner is correct that Moise teaches forming metal plugs 136 after the formation and heat treatment of capacitors as part of back end processes. Moise, however, teaches that metal plugs 136 contact plugs 114 in a FeRAM portion 103 and a region 105, not N-channel and P-channel peripheral logic transistors as in the present invention. (Col 8, lines 1-48; FIG. 1).

Thus, Moise fails to teach or suggest all limitations of independent claims 1-3, 7, and 18. Specifically, Moise fails to teach or suggest at least the following: "forming metal plugs down to active areas of a substrate after heat treating said capacitor structure," as recited in amended independent claim 1; "after said heat treating operation, forming an

[1] Based on Moise's description, it is likely that region 110 is a silicide layer. (See Col. 7, lines 35-38).

upper electrode layer in contact with said dielectric layer; and after forming said upper electrode layer, forming metal contacts contiguous to active areas of each of an N-channel and P-channel transistor in a peripheral logic area," as recited in independent claim 2; "forming a metal layer over said substrate and into said plug openings to contact said active areas after said heat is applied to said memory cell array area," as recited in independent claim 3; "after said heat treating, forming first metal conductors which contact with active areas of said N-channel and P-channel peripheral logic transistors," as recited in independent claim 7; and "forming peripheral metal plugs through said second insulating layer to contact each of said N-channel and P-channel peripheral logic transistors after said heat treating," as recited in independent claim 18.

Likewise, Jeng fails to teach or suggest at least the above noted limitations of independent claims 1-3, 7, and 18. Jeng relates to a method of fabricating DRAM devices with an array of memory cells "having capacitor-under-bit line (CUB) structures with tungsten landing plug contacts." (Col. 2, lines 38-41). Jeng teaches forming polysilicon layer to contact source/drain regions of the transistors in a memory cell area and peripheral area. (Col. 6, lines 13-53). Thus, Jeng is fails to teach or suggest forming metal plugs or contacts to any transistor, much less forming metal plugs or contacts to a peripheral logic transistor after heat treatment of a capacitor structure. Accordingly, neither Moise nor Jeng, whether considered alone or in combination, teach or suggest all limitations of independent claims 1-3, 7, and 18.

Additionally, a person skilled in the art would not have been motivated to modify the teachings of Moise based on the teachings of Jeng to provide both N-channel and P-channel transistors in the peripheral circuitry area, as asserted by the Examiner. (Office Action at 5). Jeng relates to DRAM cells and states that in addition to having N-channel access transistors, "P-channel FET's can also be provided from which Complementary Metal-Oxide-Semiconductor (CMOS) circuits can be formed, such as are *required* to the peripheral circuits on the *DRAM chip*." (Col. 5, lines 11-14)(emphasis added).

Thus, Jeng only suggests P and N-channel transistors for DRAM memory cells, volatile memory, because, according to Jeng, both P and N-channel transistors are required for DRAM peripheral circuitry. Moise, on the other hand, relates to FeRAM memory, which is non-volatile memory. Neither Jeng nor Moise teach or suggest that FeRAM cells require or would benefit from both P and N-channel peripheral logic transistors. For at least these reasons, the Applicants respectfully request the withdrawal of the rejection of claims 1-5 and 7-19.

Claims 1-7 and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee, U.S. Patent No. 6,200,855 ("Lee") in view of Moise. This rejection is respectfully traversed.

Independent claim 6 recites a "method of forming a memory device" by *inter alia* "heat treating said container capacitors," "forming N-channel and P-channel peripheral logic transistors outside said memory cell array area," and "after said heat treating, forming metal plugs to contact each of said N-channel and P-channel peripheral logic transistors through said first and second insulating layer."

The subject matter of claims 1-7 and 9 would not have been obvious over Lee in view of Moise. Lee and Moise, whether considered alone or in combination, fail to teach or suggest all limitations of independent claims 1-3, 6, and 7.

Lee relates to a method of forming semiconductor memory for reducing the contact resistance between a p+ impurity region and a metal line in a core region of the memory device. (Col. 3, lines 16-20). The Examiner asserts that Lee teaches "[f]orming peripheral metal plugs 128a through the first 108 and second 126 insulating layer to contact the N-channel *and* P-channel peripheral logic transistors." (Office Action at 7)(emphasis added). Lee, however, does not provide such a teaching or suggestion.

Lee teaches forming a metal contact only to a p+ impurity region of a transistor in a core region of the device after capacitors of the device have been formed. Lee teaches

that contacts 114c to the n+ impurity regions in the periphery are formed subsequent to the formation of the capacitors. (Col. 5, lines 35-53). Thus, Lee fails to teach or suggest all limitations of independent claims 1-3, 6, and 7. Specifically, Lee fails to teach or suggest at least the following: "forming metal plugs down to active areas of a substrate after heat treating said capacitor structure, wherein at least a portion of said metal plugs formed down to said active areas are for both N-channel and P-channel peripheral logic transistors" as recited in amended independent claim 1; "after said heat treating operation, forming an upper electrode layer in contact with said dielectric layer; and after forming said upper electrode layer, forming metal contacts contiguous to active areas of each of an N-channel and P-channel transistor in a peripheral logic area," as recited in independent claim 2; "defining multiple plug openings in material layers over said substrate at said periphery circuitry area of said substrate, wherein at least one of said plug openings exposes an active area of said transistor having said first conductivity type and at least one of said plug openings exposes an active area of said transistor having said second conductivity type; and forming a metal layer over said substrate and into said plug openings to contact said active areas after said heat is applied to said memory cell array area" as recited in independent claim 3; "after said heat treating, forming metal plugs to contact each of said N-channel and P-channel peripheral logic transistors through said first and second insulating layer," as recited in independent claim 6; and "after said heat treating, forming first metal conductors which contact with active areas of said N-channel and P-channel peripheral logic transistors," as recited in independent claim 7.

As noted above, Moise also fails to teach or suggest forming metal contacts to N-channel and P-channel peripheral logic transistors after the formation of capacitors or the heat treatment thereof. Accordingly, Lee and Moise, whether considered alone or in combination, fail to teach or suggest all limitations of independent claims 1-3, 6, and 7. For at least these reasons, the Applicants respectfully request the withdrawal of the rejection of claims 1-7 and 9.

Claims 20 and 21 stand rejected under 35 U.S.C. § 103(a) as being

unpatentable over Moise in view of Jeng and in further view of Tu et al., U.S. Patent No. 6,294,426 ("Tu"). This rejection is respectfully traversed.

Independent claim 20 recites "a method of forming a metallized contact to a periphery transistor" by *inter alia*, "after annealing said capacitor structure, etching through said second insulating layer to define a bit line opening to expose a surface of said bit line plug and etching through said second insulating layer to define peripheral plug openings in said peripheral array area to expose active areas of said first and second conductivity type" and "depositing a metal layer over said substrate to form a metal plug in said memory array area to contact said surface of said bit line plug, and form metal plugs in said peripheral array area to contact active areas each of said first conductivity type and said second conductivity type."

Independent claim 21 recites "a method of forming a metallized contact to a periphery transistor" by *inter alia*, "after annealing said capacitor structure, etching through said second insulating layer to define peripheral plug openings in said peripheral array area to expose active areas of said first and second conductivity type" and "depositing a metal layer over said substrate to form metal plugs in said peripheral array area to contact respective active areas of said first conductivity type and said second conductivity type."

The subject matter of claims 20 and 21 would not have been obvious over Moise in view of Jeng and in further view of Tu. For the same reasons discussed above in connection with independent claims 1-3, 7, and 18, Moise and Jeng, whether considered alone or in combination, fail to teach or suggest all limitations of independent claims 20 and 21. Specifically, Moise and Jeng fail to teach or suggest "after annealing said capacitor structure, . . . etching through said second insulating layer to define peripheral plug openings in said peripheral array area to expose active areas of said first and second conductivity type" and "depositing a metal layer over said substrate to form . . . metal plugs in said peripheral array area to contact active areas each of said first conductivity type and said second conductivity type," as recited in independent claims 20 and 21.

The teachings of Tu are insufficient to supplement the teachings of Moise and Jeng. Tu relates to a process for forming a CUB DRAM device and teaches forming only polysilicon plugs to contact active areas of transistors of a memory array. (Col. 3, lines 66-67; Col. 4, lines 1-14). Thus, Tu fails to teach or suggest forming a metal contact to any active area of a transistor, much less "depositing a metal layer over said substrate to form . . . metal plugs in said peripheral array area to contact active areas each of said first conductivity type and said second conductivity type" after annealing a capacitor, as recited in independent claims 20 and 21. Accordingly, Moise, Jeng, and Tu, even when considered in combination, fail to teach or suggest all limitations of independent claims 20 and 21.

Additionally, for at least the same reasons as discussed above in connection with claims 1-5 and 7-19, a person skilled in the art would not have been motivated to modify the teachings of Moise based on the teachings of Jeng to provide both N-channel and P-channel transistors in the peripheral circuitry area, contrary to the Examiner's assertion. (Office Action at 10). For at least these reasons, the Applicants respectfully request the withdrawal of the rejection of claims 20 and 21.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
Elizabeth Parsons
Registration No.: 52,499
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicants